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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/507,117	09/10/2004	Hiroyuki Takahashi	029471-0168	4725

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EXAMINER	
HUR, JUNG H	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 08/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

BK

Office Action Summary	Application No.	Applicant(s)	
	10/507,117	TAKAHASHI ET AL.	
	Examiner	Art Unit	
	Jung (John) Hur	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-51* is/are pending in the application.

4a) Of the above claim(s) *38,39 and 49-51* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,8,9,12 and 41* is/are rejected.

7)☒ Claim(s) *3-7,10,11,13-37,40 and 42-48* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 September 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/10/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *search history*.

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of Group I in the reply filed on 31 May 2006 is acknowledged. The traversal is on the ground(s) that claims 39 and 40 depend on claims 13 and 3, respectively, which are Group I claims.

First, after a further review of the claims, in the previous restriction, claim 40 should have been included in Group I, and claim 38 should have been included in Group II instead; therefore, claim 40 is herein included in elected Group I for further consideration.

In response to Applicant's traversal regarding claim 39 (which would also be applicable to claim 38, in view of the above correction and since claim 38 has a similar form as that of claim 39), the traversal is not found persuasive because claim 39 (as well as claim 38) recites "the delay circuit according to claim 13" (emphasis added), which indicates that only the delay circuit limitations from claim 13 are included in claim 39 (as well as claim 38); therefore, when compared with claim 1, claim 1 and claim 39 (along with claim 38) are restrictable, as indicated in the previous restriction requirement.

Preliminary Amendment

2. Acknowledgment is made of applicant's Preliminary Amendment, filed 10 September 2004. The changes and remarks disclosed therein were considered.

No claims have been cancelled or added by Amendment. Therefore, claims 1-51 are pending in the application. Of these, per the discussion above, claims 38, 39 and 49-51 are withdrawn from further consideration as being drawn to a non-elected invention.

Information Disclosure Statement

3. Acknowledgment is made of applicant's Information Disclosure Statement (IDS) Form PTO-1449, filed 10 September 2004. The information disclosed therein has been considered.

Specification

4. Claims 2, 3 and 12 are objected to because of the following informalities:

In claim 2, "said memory cells is a dynamic random access memory" is understood as --said memory cells are dynamic random access memory cells--.

In claim 3, "the input signal" is understood as --an input signal--.

In claim 12, "said memory cells comprise the dynamic random access memory" is understood as --said memory cells are dynamic random access memory cells--.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1, 2, 8 and 41 are rejected under 35 U.S.C. 102(b) as being anticipated by Oowaki et al. (U.S. Pat. No. 5,307,315).

Regarding claims 1 and 41, Oowaki discloses a semiconductor memory device, and a corresponding method of controlling such semiconductor device, comprising: a memory cell array (12 in Figs. 1 and 2) having a plurality of memory cells (including M1 and M2 in Fig. 2) arranged in an array from; a word line driving circuit (within 14 in Fig. 1) receiving a constant voltage (Vbw in Fig. 1, or Vwd in Figs. 2, 5 and 6) that does not depend on a provided power supply voltage (VCC in Figs. 2 and 6; Fig. 6 shows a constant Vwd for a range of VCC) as a driving voltage and driving a selected word line (WLi in Fig. 2) by the constant voltage (see Fig. 6); and a sense amplifier (32 in Fig. 1) amplifying a high level voltage of a selected bit line (for example, BL1 or BL2) to the power supply voltage (VCC; see Fig. 6).

Regarding claim 2, Oowaki further discloses that said memory cells are dynamic random access memory cells (see Fig. 2); and wherein a voltage read and amplified by said sense amplifier is written back to one of the memory cells at a time of a refresh (as a dynamic random access memory).

Regarding claim 8, Oowaki further discloses a reference voltage generating circuit (44 or 46 in Figs. 2 and 3) for generating a reference voltage (Vr1 or Vr2) that does not depend on the power supply voltage (see for example column 5, lines 37-40); and a booster circuit (including 26 in Figs. 1 and 2) for generating a constant boosted voltage (Vwd in Fig. 6) that does not depend on the power supply voltage (see Fig. 6) based on the reference voltage (see Fig. 2) and outputting the boosted voltage as the constant voltage (Vwd in Figs. 2 and 6).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Oowaki et al. (U.S. Pat. No. 5,307,315) in view of Atsumi (U.S. Pat. No. 5,394,077).

Regarding claim 9, Oowaki discloses the semiconductor memory device according to claim 1, further comprising a reference voltage circuit (44 or 46 in Figs. 2 and 3) for generating a reference voltage (Vr1 and Vr2) that does not depend on the power supply voltage (see for example column 5, lines 37-40); a booster circuit (including 26 in Figs. 1 and 2) outputting a boosted voltage (Vbw in Fig. 1, or Vwd in Figs. 2, 5 and 6), the boosted voltage that does not depend on the power supply voltage being output from said booster circuit (see Fig. 6), the boosted voltage being supplied as a power supply voltage for said word line driving circuit (as Vbw in Fig. 1), the boosted voltage being supplied to the selected word line (for example, WLi in Fig. 2) in said memory cell array, the boosted voltage supplied to the word line when the power supply voltage is reduced being kept to be the same as the boosted voltage when the power supply voltage is high (see Fig. 6), and reduction of an access speed of one of said memory cells due to reduction of the power supply voltage being suppressed (since the word line voltage is not affected by a change in power supply voltage).

Oowaki does not disclose a comparison circuit for comparing the reference voltage with a divided voltage obtained by voltage dividing the output boosted voltage; and the booster circuit receiving a result of comparison by said comparison circuit and charging a charge pump and

performing voltage boosting when the result of comparison indicates that the divided voltage is smaller than the reference voltage.

Atsumi discloses a comparison circuit (83 in Fig. 8) for comparing a reference voltage (Vref) with a divided voltage (that of N2) obtained by voltage dividing an output boosted voltage (Vccint); and a booster circuit (30) receiving a result of comparison by said comparison circuit (see Fig. 8) and charging a charge pump (within 30) and performing voltage boosting when the result of comparison indicates that the divided voltage is smaller than the reference voltage (see for example column 7, lines 4-11).

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to include a comparison circuit and a boosted voltage dividing circuit in the memory device of Oowaki (as in Atsumi), for the purpose of reducing power consumption (see for example Atsumi, column 7, lines 11-13).

9. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Oowaki et al. (U.S. Pat. No. 5,307,315) in view of Tillinghast et al. (U.S. Pat. No. 5,276,843).

Regarding claim 12, Oowaki discloses a memory device according claim 1, wherein said memory cells are dynamic random access memory cells (see Fig. 2).

Oowaki does not disclose an interface compliant with a static random access memory (SRAM).

Tillinghast discloses a dynamic random access memory comprising an interface compliant with an SRAM (see for example Abstract).

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to modify the memory device of Oowaki to include an interface compliant with an SRAM (as in Tillinghast), for the purpose of providing a less costly but higher density replacement memory for an SRAM based system (see for example Tillinghast, Abstract).

Allowable Subject Matter

10. Claims 3-7, 10, 11, 13-37, 40 and 42-48 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claims 3 and 42, the prior arts of record do not disclose or suggest a memory device as recited in claim 3 or 42, and particularly, in conjunction with other limitations, said delay circuit having a characteristic in which a delay time thereof decreases more when the provided power supply voltage is low (or lower) than when the provided power supply voltage is high (higher).

Regarding claims 45 and 46, the prior arts of record do not disclose or suggest a memory device as recited in claim 45 or 46, and particularly, in conjunction with other limitations, performing signal delay using a delay circuit having a (reverse) characteristic in which a delay time thereof decreases with reduction of the power supply voltage.

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jung (John) Hur whose telephone number is (571) 272-1870. The examiner can normally be reached on M-F 6:30 AM - 3:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

8/17/06

Jung (John) Hur
Patent Examiner
Art Unit 2824

jhh